For the elected single Species A, Figs.8,9 of the original application (No. 10/671,233) filed on 25 September 2003, what is claimed is:

1. A semiconductor vertical junction field-effect power transistor formed by a semiconductor structure having top and bottom surfaces and including a plurality of semiconductor layers with predetermined doping concentrations and thicknesses and comprising

(a) At least a bottom layer as drain layer of said transistor, a second layer as blocking or drift layer of said transistor, a third layer as channel layer of said transistor, and a top layer as source layer of said transistor;

(b) a plurality of laterally spaced U-shaped trenches with vertical side walls defining a plurality of laterally spaced mesas in said semiconductor structure; said U-shaped trenches reaching at least the interface of said blocking layer and channel layer;

(c) said vertical side walls making an angle of β with respect to the said top surface of said semiconductor structure;

(d) said mesas surrounded on the four sides perpendicular to said top surface by U-shaped semiconductor regions; said U-shaped semiconductor regions having conductivity type opposite to the conductivity type of said mesas, forming U-shaped pn junctions; the vertical side-walls of the U-shaped semiconductor regions forming vertical gate regions;

(e) the two top ends of the vertical side-walls of the said U-shaped semiconductor regions are located directly and immediately beneath the said source layer;

(f) said U-shaped pn junctions having selectively and heavily doped regions formed on the bottom of said U-shaped pn junctions for the formation of gate ohmic contacts; said

selectively and heavily doped regions having same conductivity type as said U-shaped semiconductor regions;

(g) said U-shaped junctions defining a plurality of laterally spaced vertical channel of length L_{VC} in said mesas with a uniform channel opening dimension of d_0 along the vertical channel;

(h) said top surface having ohmic contact forming the source of said transistor;

(i) said U-shaped junctions having ohmic contacts to the bottom of said U-shaped junctions forming the gate of said transistor;

(j) said semiconductor structure having ohmic contact on said bottom surface of said structure forming the drain of said transistor;

(k) said semiconductor structure having a top source layer more heavily doped than the doping densities of the vertical part of said U-shaped semiconductor regions;

2. A vertical junction field-effect power transistor according to claim **1** wherein

(a) said angle β is 90^0;

(b) said angle β is within the range of $90^0 \pm 5^0$;

(c) said angle β is within the range of $90^0 \pm 10^0$;

(d) said angle β is within the range of $90^0 \pm 20^0$;

(e) said channel opening dimension d_0 is constant along and within said vertical channel;

(f) said channel opening dimension d_0 is in the range of 0.5μm to 3μm.

(g) said channel opening dimension d_0 is within the range of $d_0 \pm 5\%d_0$ along and within said vertical channel;

(h) said channel opening dimension d_0 is within the range of $d_0 \pm 10\%d_0$ along and within said vertical channel;

(i) said channel opening dimension d_0 is within the range of $d_0 \pm 20\%d_0$ along and within said vertical channel;

(j) said channel length L_{VC} is in the range of 0.5 to 3.5um;

(k) said top source layer thickness is within the range of 0.2 to 4um;

(l) said top source layer having non-uniform doping density.

3. A vertical junction field-effect power transistor according to claim **1** wherein a buffer layer of same conductivity type is placed between said drain layer and said blocking layer first.
4. A vertical junction field-effect power transistor according to claim **1** wherein said source layer having non-uniform and increasing doping density towards the top surface of source layer of said transistor.

---------- End of Claims ----------